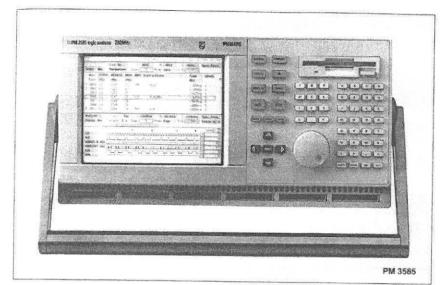
Logic Analyzers

PM 3580 Family





PM 3580 Family dual-analysis-per-pin logic analyzers

Unique dual-analysis-per-pin architecture

Combined state and timing data in a single acquisition

New user interface makes operation easier than ever

Timing analysis up to 200 MHz

State analysis up to 50 MHz

Glitch capture down to 3 ns

Choice of 32, 64 or 66 channels

Twice the information, half the work

These days, most logic analyzers seem to add to your digital analysis problem instead of helping you to solve it. They're tough to learn, and tedious to set up and operate. And if you need both state and timing data on a set of pins, you usually have to dual probe. So probes fall off. Connections loosen. And when you finally get your data, you're not even sure you can trust it. All too often, you end up thinking you'd be better off without the analyzer. So why can't the analysis of today's complex digital problems be faster and friendlier?

From now on, it can be, with the Philips PM 3580 Family. Logic analyzers that give you twice the information, half the work and none of the usual frustration.

With an exclusive dual-analysis-per-pin architecture, these instruments store state and timing data on each of up to 96 channels - in a single acquisition! No more dual probing. No more repeat measurements.

What about performance? How about timing acquisition at up to 200 MHz and state acquisition to 50 MHz, on all channels (no more trading speed for width). How about glitch capture down to 3 ns

pulses on all channels (without trading off timing resolution). Power for all your day-to-day needs - and then some for the luture. And how about operation that's faster, more intuitive and easier than ever to learn. With a modern human interface borrowing from the best of the PC industry.

How about changing your mind about logic analyzers?

The new Philips dual-analysis-perpin architecture

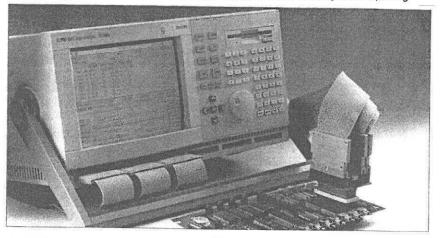
The Philips PM 3580 Family represents a radical yet affordable - step forward in logic analysis. These efficient general-purpose instruments offer state and timing capabilities powerful enough to tackle even the latest 32-bit technology. But more importantly, they give you a whole new, amazingly more effective way to work with the device under test. And that's what makes all the difference in your ability to quickly analyze your hardware and software.

Tough problems...

Consider: the classical problem in digital design. Your hardware and software both work on their own, but when you get to system integration they won't work together. The classic solution is to use a logic analyzer to check the program flow and the precise signal timing.

With old analyzers, you generally had separate state and timing sections, each with its own set of probes. Connecting one set of state probes was bad enough. But to measure the timing of a number of state signals, you had to connect a set of timing probes as well - resulting in dual probing. You had to hope they would all stay connected. And that the increased capacitive load wouldn't change the operation of your circuit.

Then came a group of logic analyzers that could switch sets of channels between state and timing analysis, allowing you to measure state, then reconfigure and measure timing for the same signals. That was great, unless you needed that same state data to define the trigger point - which is exactly usually do need. So if your analyzer had enough extra channels, you could get the information, but only by connecting a separate set of timing channels. Once again, dual probing.



Logic Analyzers

PM 3580 Family

...fast solutions

Philips' new-generation logic analyzers help you solve your digital problems - fast! Their unique dual-analysis-per-pin architecture results in the tightest coupling ever between state and timing data. One set of easy-to-connect, lightweight passive probes or adapters gives you all the state and timing information you need - in a single acquisition. Eliminating the need for time-consuming, error-prone dual probing, reprobing and uncertainty about your connections.

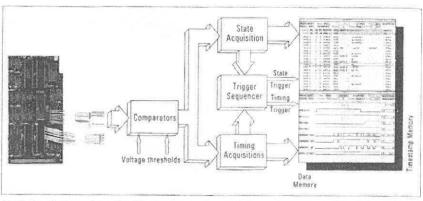
Tough problems...

Consider: the classical problem in manufacturing or service. The design works but you have a board that doesn't. And with a scope and a multimeter you can find no obvious reason why not. In an environment driven by productivity, quality and customer satisfaction, it's tempting to scrap the board. But that's a costly alternative. So as a last resort you turn to a logic analyzer.

First you have to learn, or relearn, how the instrument works. And hope you're lucky enough to have found all the manuals. Then you connect up all the probes, and try to set up the analyzer to capture the data you need. When you find a program error, you need to see the exact timing data between the state clocking moments. So you move the probes, set up the analyzer again, and so on and so on. Altogether, a long and frustrating task.

...fast solutions

It doesn't have to be so difficult. By truly integrating state and timing analysis, the basic operation of the PM 3580 Family logic analyzers is so simplified that it can be learned in less than 30 minutes. Then, within minutes, you can set up the analyzer, make a single acquisition and be analyzing your data all the state and timing data you need. And with built-in floppy disk drive and



The 'dual-analysis-per-channel' architecture, repeated for each logical analyzer in PM 3585 systems.

functions like compare for Go/NoGo testing, the PM 3580 logic analyzer is no longer an instrument of the last resort but an essential tool for manufacturing and service.

In brief, Philips' unique dual-analysis-per-pin architecture gets you up and running faster. And gives you data you can rely on. All with less fuss and frustration. Now that's new!

Dual-analysis channels go further

When you choose a Philips PM 3580 Family logic analyzer, remember that you need fewer channels than with a conventional logic analyzer. For example, if you were working with an 80286-based system using a conventional analyzer, you would need 48 channels for state analysis plus, say, another 32 for timing analysis - a total of 80 channels.

With a 64-channel PM 3580, 48 channels are all you need for the essential state and timing analysis of an 80286. You'd still have another 16

channels for acquiring other data - timing analysis of glue logic, for example. Or for state and timing analysis of an external bus!

With a 96-channel PM 3585, you can acquire all the state and timing information you need (for example, for disassembly and bus timing) from most advanced 32-bit microprocessors, and still have 16 channels left over for the glue logic!

The Philips new-generation logic analyzers

Whether you are debugging simple digital circuits or developing state-of-the-art systems, one of the PM 3580 Family analyzers will help you solve your problems:

PM 3580/30 - 32 dual-analysis channels with 100 MHz timing and 50 MHz state

Logic analysis at its affordable best. The base model offers efficient handling of basic logic timing measurements and 8-bit microprocessor applications.

PM 3580/60 - 64 dual-analysis channels with 100 MHz timing and 50 MHz state

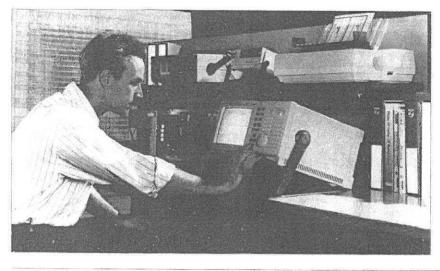
More channels let you test more sophisticated circuitry. This model is suitable for logic timing measurements on 8- and 16-bit microprocessors.

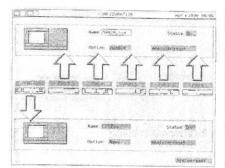
PM 3585/60 - 64 dual-analysis channels with 200 MHz timing and 50 MHz state

This high-performance instrument can be divided into two logically separate analyzers with 16-channel sections - giving you multiprocessor analysis capability. Use this model for high-resolution logic timing measurements or 8- and 16-bit microprocessor applications.

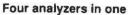
PM 3585/90 - 96 dual-analysis channels with 200 MHz timing and 50 MHz state

This top-of-the-line model offers the same capabilities as the PM 3585/60, plus the additional capability to handle 32-bit processors.





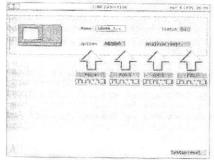
Assign any of the available pods to either logical analyzer on the PM 3585.



With PM 3585 models, you get state and timing analysis on every channel. *Plus*, the ability to split the instrument at any 16-channel section into two logically separate analyzers.

Each analyzer can measure state data using a full set of external clocks. And, of course, record all the associated timing data on the same channels. All tightly correlated down to 5 ns accuracy. That's four discrete analyzers in one instrument!

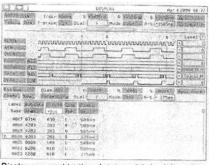
Each analyzer contains its own data labels and its own fully functional trigger sequencer. The



Just read-in the standard microprocessor set-up from floppy disk, and press RUN.

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Then scroll to the noisy bus transition and zoom to fill the display...



Display any combination of state and timing information from either analyzer.

links between the sequencers are so tight that they can trigger or wait for each other (or for an external signal) at any trigger level.

State and timing can even be stopped independently without losing time correlation - particularly useful if you want to capture events widely separated by time.

Suppose you have a multi-bus system - a microprocessor and a peripheral bus. The processor sends a sequence to the peripheral, then waits for a response. When it comes, the response isn't quite what you expected. What next?



All the standard 68000 labels are visible on the display. If you see something wrong...

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So zero-in on the source of the problem by simply toggling through the address lines to see which ones are noisy. This display reveals a 10 ns oscillation.

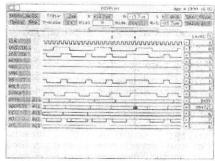
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99/1 99/23 96/23	8788 414 1 52845 6788 414 1 76846 5288 618 1 57546		

An overview is available showing the time relationships between the various sets of data acquired.

With a PM 3585/90, you could select 64 dualchannels to monitor the microprocessor and the remaining 32 to track the peripheral bus. You have two logically separate analyzers to follow the sequence being sent and received at each stage of the complex data transfers, which can help you determine whether it's the board or the peripheral that has the problem.

The logical analyzers

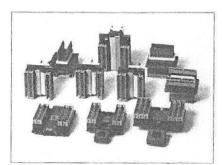
In logic analysis, you're the real 'analyzer'. The main function of the 'logic analyzer' is to provide you with the data you need, in the form in which you need it. And it should perform that task



... just switch-over to see the actual signal timing for the same labels. This display shows a noisy address bus transition.



So zero-in on the source of the problem by simply toggling through the address lines to see which ones are noisy. This display reveals a 10 ns oscillation.



Quick-connect microprocessor pods have eliminated the 50 or 60 separate connections which formerly had to be made manually to connect the logic analyzer to the target system.

quickly, competently and efficiently. Leaving you free to study the data, not the operating manuals.

The PM 3580 Family logic analyzers give you unprecedented flexibility to display the data you need in the form you need it. Without requiring you to be a keyboard wizard.

Getting started guickly

For example, if you're working with a 68000 microprocessor, you just clip onto the chip, load the standard channel settings from a floppy disk and press 'RUN'. The analyzer triggers on a default 'Don't care' condition and your data appear on the screen. It's that simple. Then select a trigger condition from a standard list to zoomin on a specific area of interest.

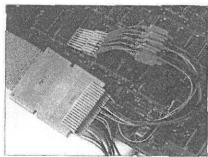
All the data you need

You can toggle between state and timing data for all the signals and buses - thanks to the dual-analysis-per-pin architecture, you automatically get both. All with just a single set of connections and a single set-up. With most conventional logic analyzers, you would have to clip-on a few extra high-speed probes to get your timing data, since quick-connect adapters are usually limited to state analysis.

Now, when your state list shows something unexpected, you can switch right to the timing data to look for the cause, as shown in the example as on page 6-5

A user interface that won't leave you guessing

Here's just how intuitive the PM 3580 analyzers can be. If you want to view the processor clock right next to the address bus in the timing diagram, simply move the cursor down to the address label, press INSERT and a pop-up menu offers you a list of labels to choose from. Type 'C' for 'Clock', and you have it. Right where you want it. Or if you want to delete a signal, just press DELETE.



Lightweight passive probes and low-capacitance microprocessor adapters minimize loading of your test circuit - a factor that can often affect its behaviour with conventional logic analysis probes.

Whenever you need them, pop-up menus will remind you of the available choices. So even if you don't use a logic analyzer regularly, you won't be left guessing.

And when you know exactly where you want to be, you'll find the PM 3580 short cuts are even faster. For example, you can type 'T' to move the display directly to the trigger point, without needing to call-up a menu.

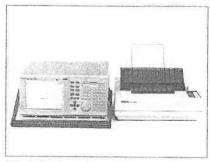
Setting-up measurements has never been so simple

Powerful and friendly data analysis functions are only part of the PM 3580 story. In most cases, you want to customize data acquisition to your application. By labelling data so that it relates to your circuit - for example defining clocks, interrupt lines and buses. And by using the trigger power of the logic analyzer to zoom-in on the data you are interested in.

With the PM 3580 Family analyzers, entering data labels is as easy as typing the name and specifying one or a group of channels. With the full alphanumeric keyboard, even a whole list of labels can be entered quickly and conveniently. While with the optional microprocessor support packages, labelling is handled fully automatically.

Synchronous (state) clock definition is done in exactly the same way. External clocks can be selected from any of the data channels, and can be qualified by any (or all) channels. And whenever a synchronous clock is defined, the analyzer automatically monitors state data - fully time-correlated with the timing information.

Once you have defined the data labels, you can view them in both state and timing displays. Even at the same time, if you want, in split-screen mode. You can also 'post-define' labels after you've made an acquisition (for example if you want to split a bus).



With a built-in Centronics parallel printer port, it's easy to make hard-copy output from the PM 3580 Family logic analyzers.

As well as acquiring sate and timing data on all channels at once, Philips' new dual-analyzer-per-channel architecture also gives you a simpler, single trigger sequencer. Traditional analyzers have separate sequencers for state and timing data acquisitions, with only loose links, if any, between them. The sequencers of the PM 3580 Family offer 8 levels, which may contain a mixture of state and timing trigger events, all organized in a easy-to-read, Englishlanguage style. Trigger words are arranged in the same way as your data labels, for easy interpretation of your results.

Trigger set-up couldn't be easier. Just select from a predefined list of the most commonly used trigger sequences, enter the trigger words, and hit 'RUN'

For more sophisticated triggering, you can switch to 'user-defined' mode. Start from scratch, or use a predefined sequence as a starting point - as you prefer. Select patterns, ranges, time-filters and more - all in a single sequence. And any level can wait for, and/or send, an external trigger pulse.

Easy-to-use no longer means compromising on performance

With the PM 3580 Family analyzers, easy-touse doesn't mean limited performance. Just take a look at the specifications of these advanced instruments. Like 100 or 200 MHz timing acquisition with transitional storage. On all channels, all the time. Plus 50 MHz state acquisition at the same time - remaining at 50 MHz, no matter what you're doing. And glitch capture down to 3 ns, again on all channels. With no trade-offs in timing resolution.

Or take data memory. You get a full 2K per channel on the PM 3585 (1K on the PM 3580). Separate from the timestamp memory, for storing states, timing data or both as required by your application. With both state and timing data whether stored or not - available at all times for triggering the analyzer.

So with Philips dual-analysis-per-pin architecture, the PM 3580 Family provides two powerful logic analyzers. Merged into a single instrument, with double the logic analysis power.

That power goes right down to the probe tipswith all-new lightweight, passive probes and lowcapacitance microprocessor adapters. Minimizing loading of your test circuit - a factor that can often affect its behaviour with conventional logic analysis probes. Circuit loading is a particularly important consideration if your design uses the latest in microprocessor technology, or pushes component performance to the limits.

Increasing the confidence factor

The PM 3580 Family logic analyzers are built for the long-term reliability you demand from your instrumentation. The use of semi-custom ASIC technology means a reduced parts count, and more value-for-money. The entire logic analyzer circuitry resides on a single board - even for the most advanced 96-channel/200 MHz version - complete with CPU, parallel printer interface, connector for an external VGA monitor and an RS232 port for diagnostics (and future options). And it's all assembled using the latest in production technology.

Each model also performs an automatic selftest sequence and a de-skew procedure on all channels, each time you power it up. And if it should ever develop a fault, its 'design-for-service' construction helps the service engineer to get it up and running again in minimum time and at minimum cost.

Quality during the entire lifetime of the instrument is guaranteed thanks to the extensive Boundary Scan Test (BST) facility which is built into every unit. This enables the functioning of the entire analyzer to be verified down to component level, in a minimum of time, and without requiring external equipment.

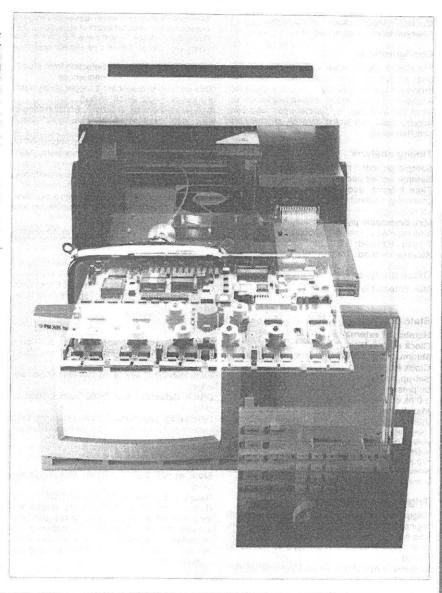
All the tools you need

The PM 3580 analyzers are supplied as standard with a full set of lightweight 200 k Ω , 7 pF passive probes. These can be disconnected at various stages from probe tip through to the front panel connector on the analyzer. Like when you want to leave a set of probes connected to one target while you are working with another. To help you make those connections to the target, a wide range of clips is available.

The PM 3580 also comes with a whole new range of optional microprocessor adapters with the lowest capacitance you'll find anywhere (in fact, they're the first quick connection adapters for measuring both high speed timing and state signals simultaneously. So if your circuit works, it'll continue to work when you connect your PM 3580 analyzer. And if it doesn't work, connecting the analyzer won't conceal the problem.

An ever-increasing range of easy-to-use disassembly software is also available, covering most popular microprocessors.

For maximum convenience, all probes, together with a set of user documentation, fit easily into the attractive accessory pouch (supplied as standard), which is integrated with the front cover of the analyzer. And while the PM 3580 analyzers are in themselves extremely light and portable, an optional cart makes it even easier to move them around the lab, together with a printer and paper, for example.



1991 Fluke and Philips Catalog

Specifications

Technical Specifications

Input Section

Probe impedance: 200 k Ω /7 pF (Typ.) Thresholds per 8 ch.: TTL, ECL or variable (-3.0 V, +12.0 V)

Threshold accuracy: 150 mV or 3% of selected threshold value, whichever is greater Minimum input overdrive: 250 mV or 25% of

swing, whichever is greater Minimum swing: 500 mV

Maximum input voltage: ±50 V peak Channel to channel skew: <4 ns

Configurations

PM 3580 analyzers have a single analyzer with dual-analysis-per-pin architecture. PM3585 analyzers can be split into 2 logically separate analyzers. Each analyzer can be assigned any or all of the available 16 channel pods, and can acquire state and timing data on all channels simultaneously.

Timing analyzer

Sample period: 5 ns (10 ns for PM 3580)
Sample period accuracy: 0.005%
Time interval accuracy: ±(Sample period +

Time interval accuracy: ±(Sample period + channel to channel skew +0.005% of time interval reading)

Min. detectable pulse:

6 ns (typical) (11 ns for PM 3580) 7 ns (guaranteed) (12 ns for PM 3580) Storage method: Transitional

Glitch analyzer

Min. detectable glitch: 3 ns (typical) 4 ns (quaranteed)

State analyzer

Number of external clocks: 4¹ Clock edges: Rising, falling or any Minimum clock width: 5 ns

Clock Repetition Rate: 50 MHz maximum Set-up, hold time: Data and clock qualifiers must be present >10² ns before, and remain present ≥ 0 ns after, the external clocking signal.

Max. time-stamp error: ± (5 ns + 0.005% of time interval reading)

Selectable from any channel. Clock qualifier expressions defined by ANDing any/all input channels; up to 4 such expressions can be 0Red together. ²To support individual micrprocessors, set-up and hold

4To support individual microrocessors, set-up and hold times are adapted as necessary to support the maximum processor speed.

Trigger sequencer

Trigger sequencer for PM 3580 and for each logical analyzer in PM 3585. Note that all state and timing trigger recognizers are always available, even when that data type is not being stored.

Sequence type: Pre-defined, User-defined, Restart.

Data Memory Storage Modes

Data memory on the PM 3580 Family is separate from the timing memory. State data are always time-stamped.

and the second s	PM	3585	PM3580		
	No. of states	Timing data length ³	No. of states	Timing data length ³	
Timing/State ⁴	1024	5.12 µs/12 hrs	512	5.12 μs/6 hrs	
State only	2048		1024	-	
Timing only ⁵	-	10.24 µs/24 hrs	-	10.24 µs/12 hrs	
Timing/Glitch		5.12 µs/12 hrs	III.	5.12 µs/12 hrs	

Minimum measurement length applies for signal rates > 25 MHz. Maximum measurement length applies for very slow input signals.

Maximum time-correlated length of state data: 2 days
* Timing/State storage: Default if external clock is defined

5 Timing only storage: Default if no external clock is defined

Pre-defined sequences: Selection from standard list of commonly used sequences

User-defined sequences: 8 trigger levels each of 2 trigger conditions (If, else if)

Restart sequences: 8 single condition trigger levels with global restart condition

Level to level delay: None

Trigger conditions: Any ORed combination of either state or of timing trigger recognizers, (NOT recognizers are first ANDed) or timeout counter. On satisfying a condition, control is passed to any other trigger level.

Acquisition halt: State or timing data acquisition can be independently halted on satisfying any trigger condition.

Counters: A total of 4 counters (1 - 65535) are available for use in any trigger condition as event or timeout counter.

Trigger recognizers

Each recognizer (except Glitch and Edge) uses an ANDed combination of bit values (0,1 or X) for all defined labels.

Timing

Timing words: 1 high speed word (resolution = sample period + skew); 2 with timing filters (20 ns - 1.31 ms)

Edge detector: Any 0Red combination of any edges

Glitch detector: Any 0Red combination of glitches

Glitch/Edge triggering: Isolated or during valid pattern which has been present for a minimum

State

State words: 8 (or 6 if timing filter words are used)

Range recognizers: Range or NOT range. Range is defined as AND of range recognizers for a number of labels. Up to 32-bits per label allowed. Maximum 1 label per 16 channel group Immediate recognizers: Each pair of state words (w1:w2, w3:w4 etc.) can be used to recognize adjacent words

Timeout counter: 20 ns - 65535 ms

Trigger positions: Predefined positions: Beginning, Beginning +25%, Center, End-25% or End of acquired state and timing data. Additionally, state and timing can each be arbitrarily delayed with respect to the trigger point in percent of memory, time (to a maximum of 65536 ms) or clocks (state only).

External triggering: Each trigger level can trigger and/or be triggered by an external instrument (via BNC) or the other logical analyzer in the PM 3585.

Selective State Storage

Selective State Storage can be specified, either globally or per individual level, prior to the trigger point, using any ORed expressions of the following: Anystate, Nostate. State word, NOT state word, Range, NOT range, Qualified external clock.

Acquisition Functions

Single: RUN key starts, Trigger sequencer or STOP key stops.

Auto-repeat: RUN key starts. Acquisitions repeated

indefinitely at programmed intervals.

Auto-repeat stop: STOP key, Compare/Non-compare

Auto-repeat delay: 1 s to 65535 s

Status display: If the analyzer does not trigger within 1 sec of starting an acquisition, a status pop-up appears indicating the progression through the trigger levels.

Note: Each acquisition is time stamped with the absolute time of the measurement (trigger point)

Logic Probing

Dynamic indication of signal status on all lines: High, low or changing

Label formatting and attributes

Label names: Up to 8 character name defining signals or logical groups of signals (busses)

Max. no. channels/label: 32

Max. no. labels: 120

Label attributes: Validity for clocks, Inhibit timing data acquisition

Microprocessor Support

Ordernumber	Processor	Package	Max.Freq.'	Pods ² Disa/Full	Modes ³ S/T	Accessories
PF 8610/30	8085	DIP-clip	6	2/3	S/T	
PF 8614/30	Z80	DIP-clip	10	2/3	S/T	
PF 8620/30	68000/10	DIP-clip	16.67	3/4	S/T	
PF 8620/31	68000/10	DIP-skt.	16.67	3/4	S/T	PF 8620/81
PF 8620/32	68000/10	PLCC	16.67	3/4	S/T	PF 8620/82
PF 8620/33	68000/10	PGA	16.67	3/4	S/T	PF 8620/83
PF 8624/30	8086/88	DIP-clip	10	2/3	S/T	
PF 8625/33°	80186/88	PGA	16	2/4	S/T	PF 8625/83
PF 8626/32	80286	PLCC	25	3/4	S/T	PF 8626/82
PF 8626/33	80286	PGA	25	3/4	S/T	PF 8626/83
PF 8627/32°	80186/88EB	PLCC	16	2/5	S/T	PF 8627/82
PF 8630/33	68020	PGA	33.33	5/6	S/T	PF 8630/83
PF 8635/33 ^s	386™ DX	PGA	33.33	5/5	S	PF 8635/83

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Ordernumber	Processor	Package	Max.Freq.'	Pods²/Full	Modes ³ S/T	Accessories
PF 8611/20	6800/02/08	DIP-clip	2	3	S/T	
PF 8612/20	6809/E	DIP-clip	2	3	S/T	
PF 8615/20	8031/51	DIP-clip	18	3	S/T	
PF 8616/22	68HC11	PLCC	2.1	3	S/T	PF 8616/82
PF 8620/20	68000/10	DIP-clip	16.67	4	S/T	
PF 8620/21	68000/10	DIP-skt.	16.67	4	S/T	PF 8620/81
PF 8620/22	68000/10	PLCC	16.67	4	S/T	PF 8620/82
PF 8620/23	68000/10	PGA	16.67	4	S/T	PF 8620/83
PF 8626/22	80286	PLCC	25	4	S/T	PF 8626/82
PF 8626/23	80286	PGA	25	4	S/T	PF 8626/83
PF 8634/23°	386™ DX	DXPGA	33.33	6	T	PF 8635/83
PF 8636/23°	i486™	PGA	33.33	6	T	PF 8637/83
PF 8644/23 ⁵	i960 CA	PGA	33.33	6	Т	PF 8645/83

Final values for other processors were not available at the time of printing. Consult factory for the latest data.

Adaptor loading is typically 15 pF. For the 68000/10. 68HC001, 68HC11, 68020, 6800, 6809, 8085, 80286, and Z80 all signals are 200 $K\Omega/15$ pF except: 68000/10, 68HC001: UDS, LDS -100 KΩ/25 pF (Typical) A0 · 67 KΩ S0, S1, RESET, PEACK 150 KΩ.

68001: 80286:

25 pF (Typical) NOT LIR - 67 KΩ

68HC11:

All address lines - 20 pF (Typical)

Microprocessor adaptor accessories

Order number Description PF 8616/82 68HC11 PLCC 15 mm extension socket 68000/10 DIP 4 mm extension PF 8620/81 sockets (set of 3) PF 8620/82 68000/10 PLCC 15 mm extension socket PF 8620/83 68000/10 PGA 4 mm extension sockets (set of 3) PF 8625/835 80186/88 PGA 4 mm extension sockets (set of 3) PF 8626/82 80286 PLCC 15 mm extension socket PF 8626/83 80286 PGA 4 mm extension sockets (set of 3) PF 8627/82⁵ 80186/88EB PLCC 15 mm extension socket 68020 PGA 4 mm extension PF 8630/83 sockets (set of 3) PF 8635/83 i386™ DX PGA 4 mm extension sockets (set of 3) PF 8637/83 i486™ PGA 4 mm extension sockets (set of 3) PF 8645/83⁵ i960™ PGA 4 mm extension

Custom Disa Development Software

PF 8629/305: Enables fast, simple generation o disassemblers for microprocessors (up to 32-bi busses) and equivalent applications (See separate datasheet for details).

sockets (set of 3)

Notes:

1. Maximum frequency is maximum processor frequenc available at time of printing, or the maximum frequenc supported by the PM 3580 family, whichever is lower Please consult sales office for latest information. 2. Pods Disa/Full refers to the number of channel

required for disassembly only and for full timing analysis Modes: Adapters can acquire both state and high speed timing data (S/T), state data and low-resolutio timing data (S), or high-speed timing data only (T). 4. 386 DX and i486 are trademarks of the Intel Corp.

5. Available Feb. 1991.

Data display

Display modes: Single screen or dual screen. Each screen section can contain data of any type or source

Data type: Timing waveform or State list

Data source: New measurement, Reference measurement or comparison of New and Reference Measurement

Display labels: Any labels defined in FORMAT, displayed in any order. Also time relative to trigger point and/or time-difference and clock (state lists)

Level display: Current levels in trigger sequence are displayed

Measurement cursors: R and S

Dial functions: Scroll, set R-cursor, set S-cursor, set Time/division, set vertical scale

Dial mode: Movement on each dial-click: Scroll, Edge, Trigger level, Division, Page, Glitch, Find pattern

Find pattern (state): Any bit-mask, defined by label

Time/Division (timing): 3 steps per decade from 5 ns to 50 ks

Co-scroll: Data in dual screen display can be scrolled synchronously with user-defined timeoffset

Data/Settings Storage

DOS-format 2.0 MByte (1.44 MByte formatted) 3.5" floppy disk. Will also accept externally formatted 720 kbyte disks.

Hardcopy Output

Epson and Epson compatible printers via Centronix parallel printer output

External Video Output

VGA compatible video output socket (mono-chrome)

External BNC Trigger

Active trigger level: High Input resistance: 100 KΩ

Minimum pulse width: 25 ns (typical)

External BNC Trigger Out

Active trigger level: High Output Impedance: 50Ω Pulse width: 20 ns (typical)

Delay between trigger condition true (at probetip) to triggerout true: Approx. 430 ns

General Specifications

Display: 9"monochrome screen with 4-level greyscale

Dimensions: Excluding handle (8.7" x 16.6" x 14.2") 220 mm high x 420 mm wide x 360 mm deep. Handle in carrying position (8.7" x 18.2" x 19.0") 220 mm high x 462 mm wide x 482 mm deep

Weight (approx.): 13 kg (28.7 lbs) Power: 140 VA (105 VA for PM 3580)

Environmental Data

Standards: MIL-T-28800 D, Type III, Class 5, Style E

Temperature:

- Rated range of use: 5°C to 40°C (41°F to 95°F)

- Limited range of operation: 0°C to 55°C (32°F to

- rangé of storage and transport: -40°C to 70°C (-40°F to 158°F)

Relative Humidity: operating: 15% to 90% non condensing

- storage and transport: 5% to 95% non condensing

Altitude:

operating: 4500 m (15.000 ft)

- storage and transport: 12000 m (40.000 ft) **Vibration:** Swept sine resonance search, 5-55 Hz, 2g (peak), 15 minutes per axis, 10 minutes resonance dwell

EMI: VDE 0871 Class B, FCC A

Safety designed to meet: IEC 348 Class 1, VDE 0411, CSA 556B

Note: These data do not apply to the disk media.

Ordering Information

Family Overview

PF 8690/00

Model number	PM 3580/30	PM 3580/60	PM 3585/60	PM 3585/90
State/Timing channels	32	64	64	96
16 channel pods	2	4	4	6
Timing Speed (MHz)	100	100	200	200
State Speed (MHz)	50	50	50	50
Data memory (Kb/ch.)	1	1	2	2
32-channel upgrade	PF8652/20	_	PF8652/25	
2 years extra return- to-depot warranty	PM 3580/39	PM 3580/69	PM 3585/69	PM 3585/99

Note: Mainframes are delivered with a complete set of logic pods and front cover with integrated accessory pouch and manuals.

Various options and accessories

Extra English manual set +

system software

Order number	Description	PF 8690/10	Extra French manual set +
PF 8600/20	16-channel Logic Pod, complete	O E GARDAN MA	system software
PF 8600/21	16-channel Pod cable	PF 8690/20	Extra German manual set +
PF 8600/22	16-channel probe set, including		system software
	shroud	PM 8819/2035	Measuring clips (black, full-size)
PF 8600/24	40 Mini-measuring clips (grey, low-profile)	PM 8819/3050	Mini-measuring clips (red, dual pin)
PF 8603/20	16-channel RC compensated connectors (set of10)(Enable	TC 100	Cart for PM 3580/PM 3585 with 2 extra shelves
	direct connection of pod cable to	PM 8902/00	12 V DC/AC Convertor
	circuit)	PM 8903/00	12 V DC/AC Convertor + acces-
PF 8666/20	Extra front cover with integrated accessory pouch		sories